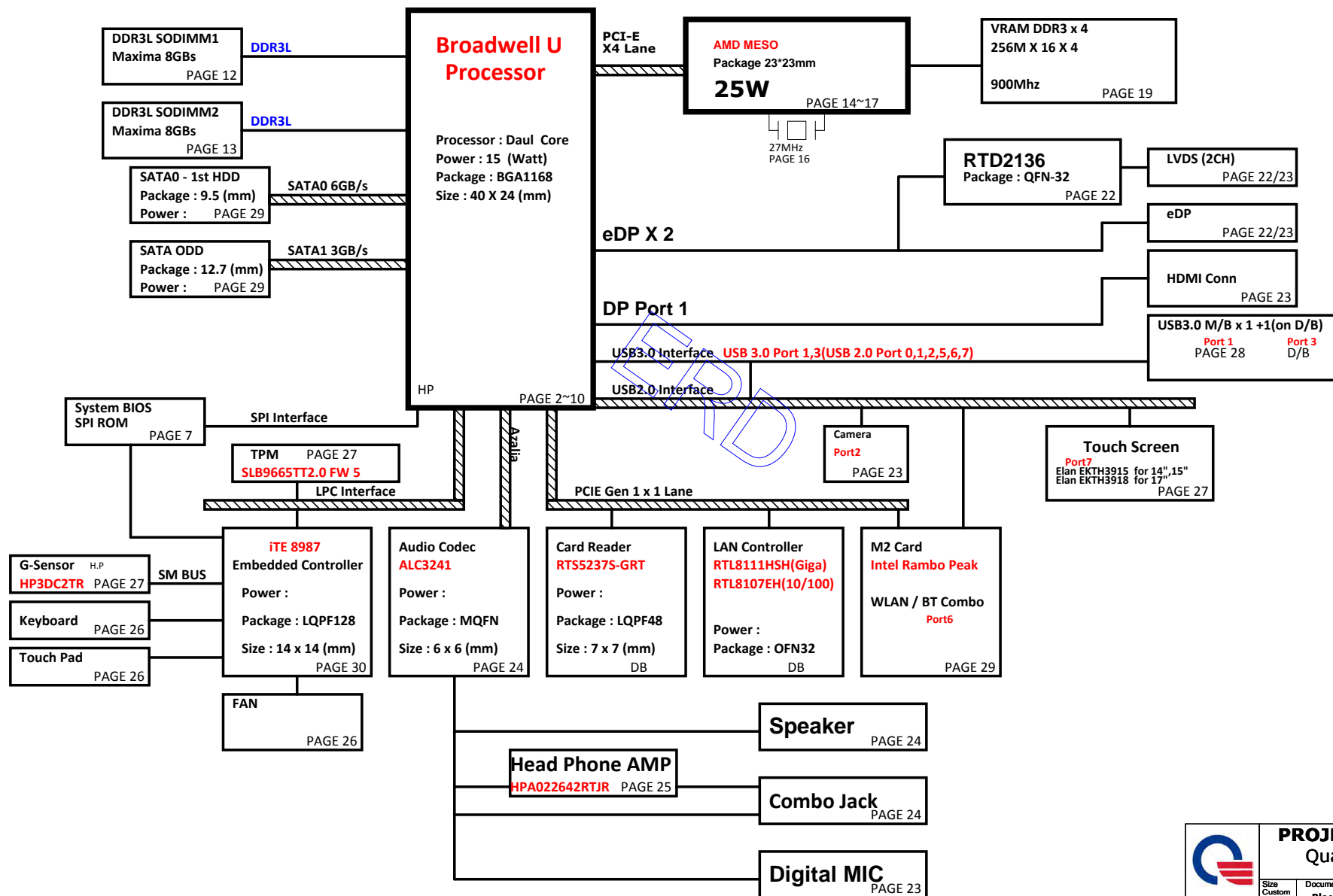


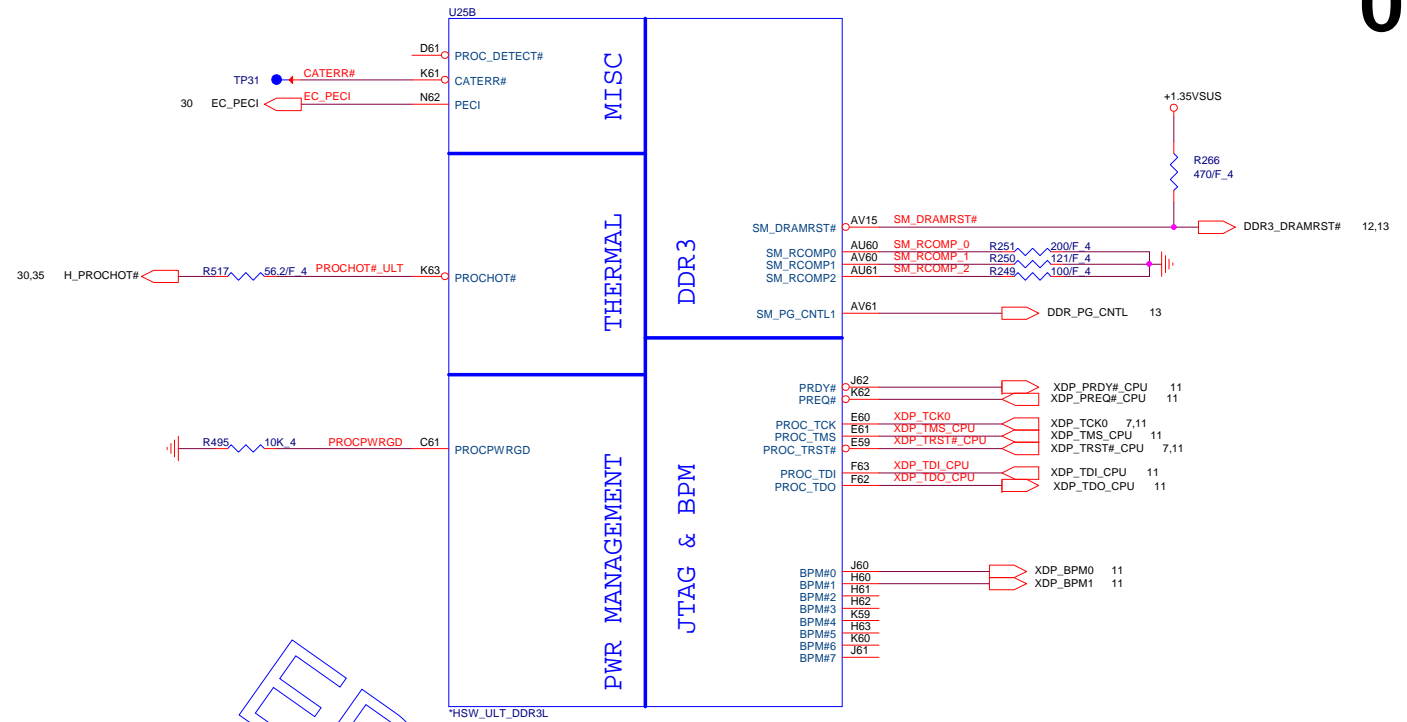
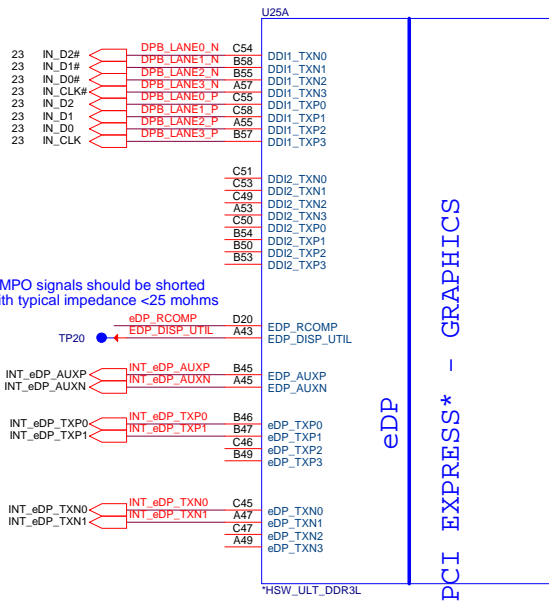
X11 DIS (14" / 15" / 17") Chocolate X11 Intel Crescent Bay ULT Platform Block Diagram



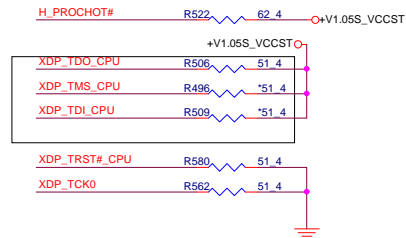
PROJECT : X11
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Monday, January 05, 2015	Sheet	1 of 40

Note
VGA/CPU need check PW

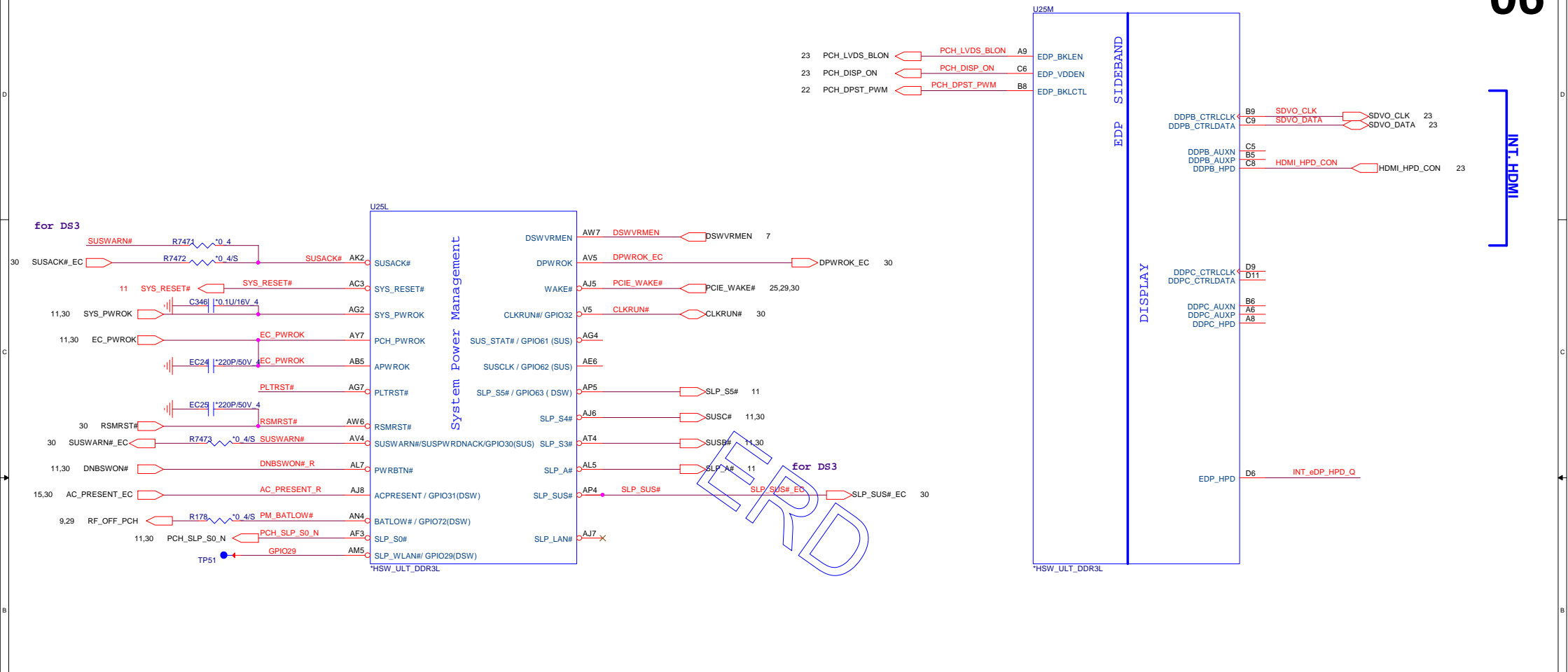


Processor pull-up (CPU)

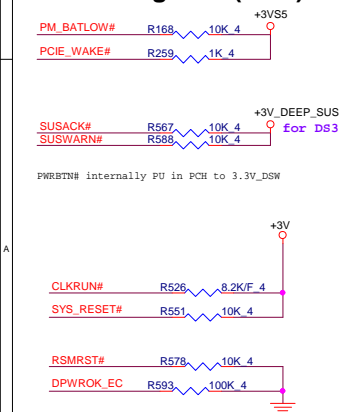


[illegible]

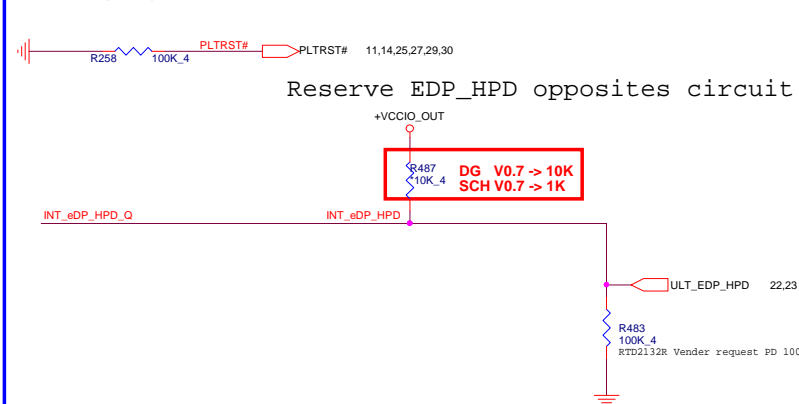




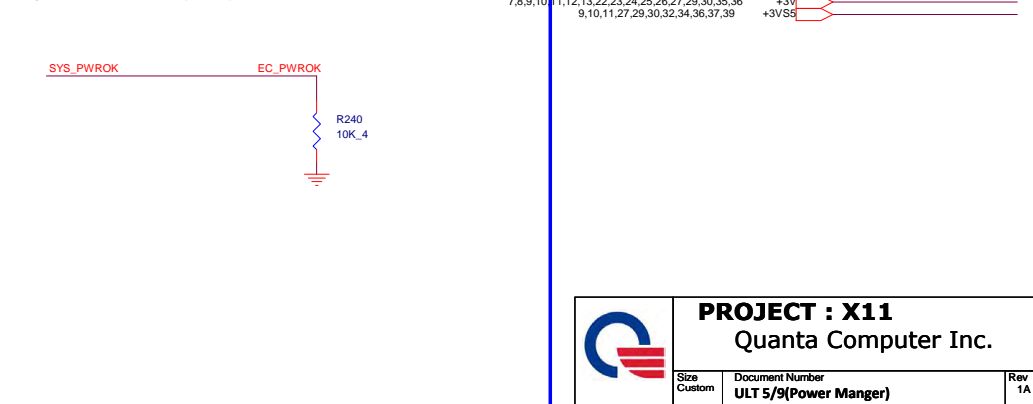
PCH Pull-high/low(CLG)



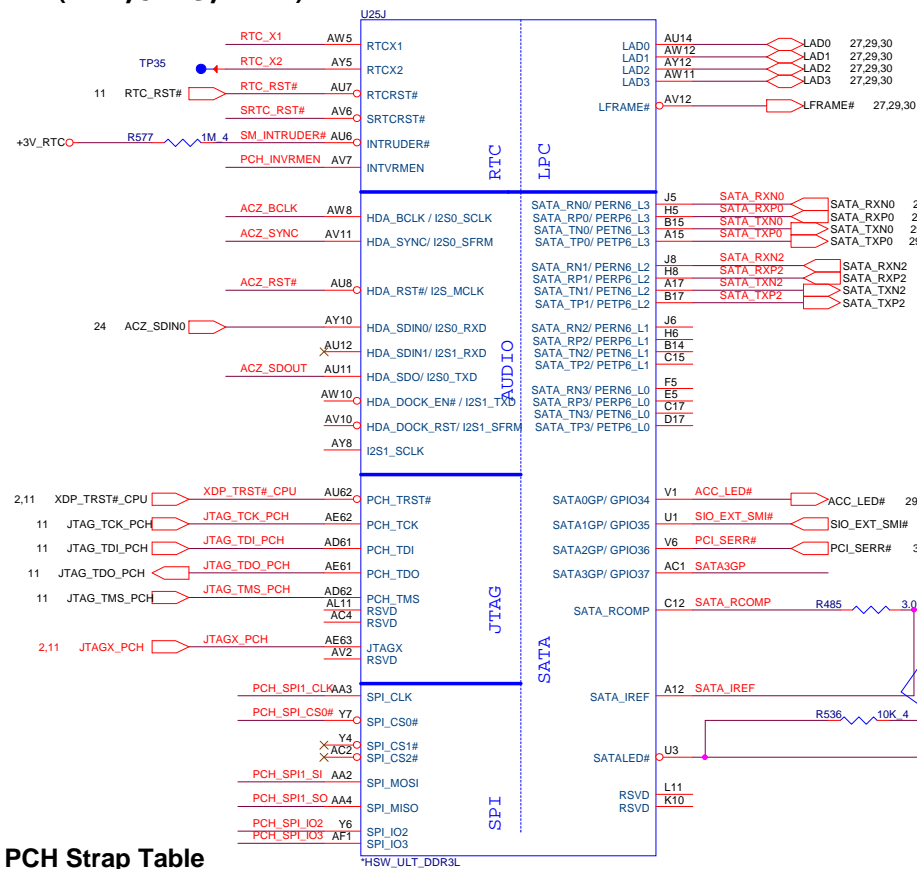
PLTRST#(CLG)



System PWR_OK(CLG)



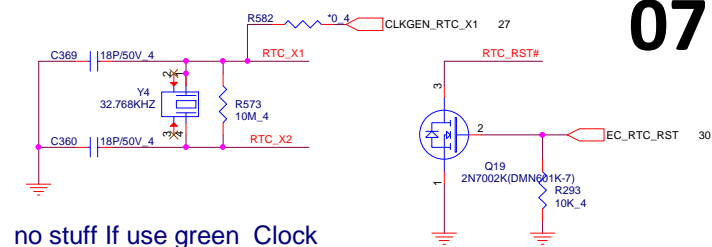
Lynx Point-LP Platform Controller RDHub
(HDA,JTAG,SATA)



PCH Strap Table

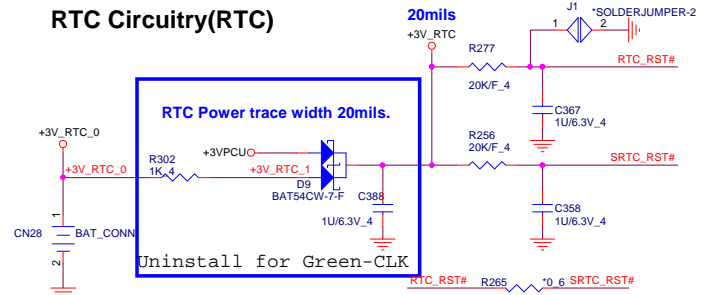
Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	+3V_RTCO—R575—330K 4 PCH_INVRMEN						
GPIO_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	30 GPIO33_EC R581—1K 4 ACZ_SDOUT
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTCO—R576—330K 4 DSWVRMEN 6						
				<div><div>30</div><div>PCH_SPI_CS0#_R</div><div></div><div>PCH_SPI_CS0#_R</div><div>30</div><div>PCH_SPI1_CLK_R</div><div></div><div>PCH_SPI1_CLK_R</div><div>30</div><div>PCH_SPI1_SI_R</div><div></div><div>PCH_SPI1_SI_R</div><div>30</div><div>PCH_SPI1_SO_R</div><div></div><div>PCH_SPI1_SO_R</div></div>						

RTC Clock 32.768KHz	
---------------------	--

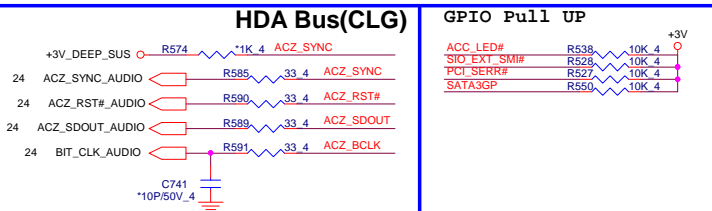


no stuff If use green Clock

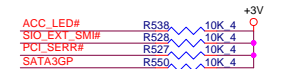
RTC Circuitry(RTC)



HDA Bus(CLG)

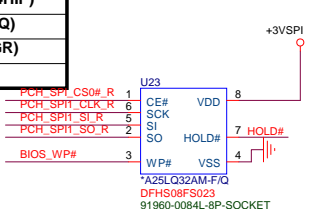


GPIO Pull UP



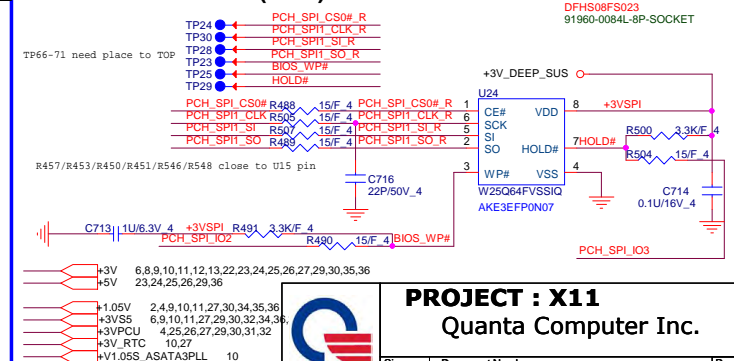
Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket



U23&U24 footprint 要重疊

PCH SPI ROM(CLG)

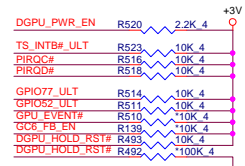


PROJECT : X11
Quanta Computer Inc.

Size Custom	Document Number ULT 6/9(SATA/HDA)	Rev 1A
Date: Tuesday, January 06, 2015	Sheet	7 of 40

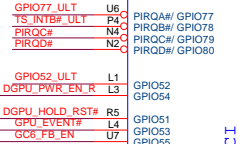
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

PCI/USB0C# Pull-up(CLG)

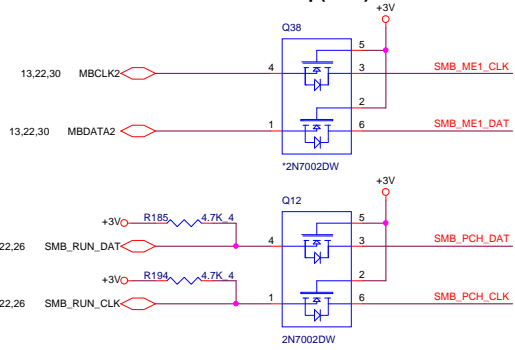


SMBALERT#	R186	10K 4
USB_OC1#	R195	10K 4
USB_OC2#	R211	10K 4
USB_OC3#	R561	10K 4
USB_OC4#	R571	10K 4

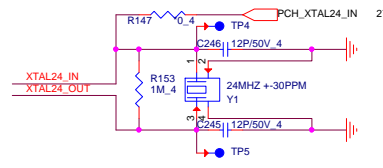
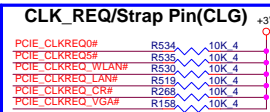
USB3.0 M/B



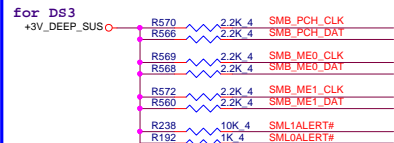
SMBus/Pull-up(CLG)



SMBus/Pull-up(CLG)



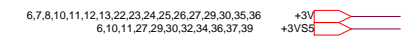
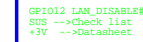
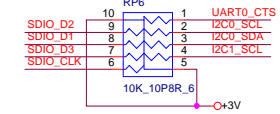
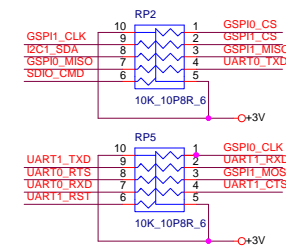
SMBus/Pull-up(CLG)



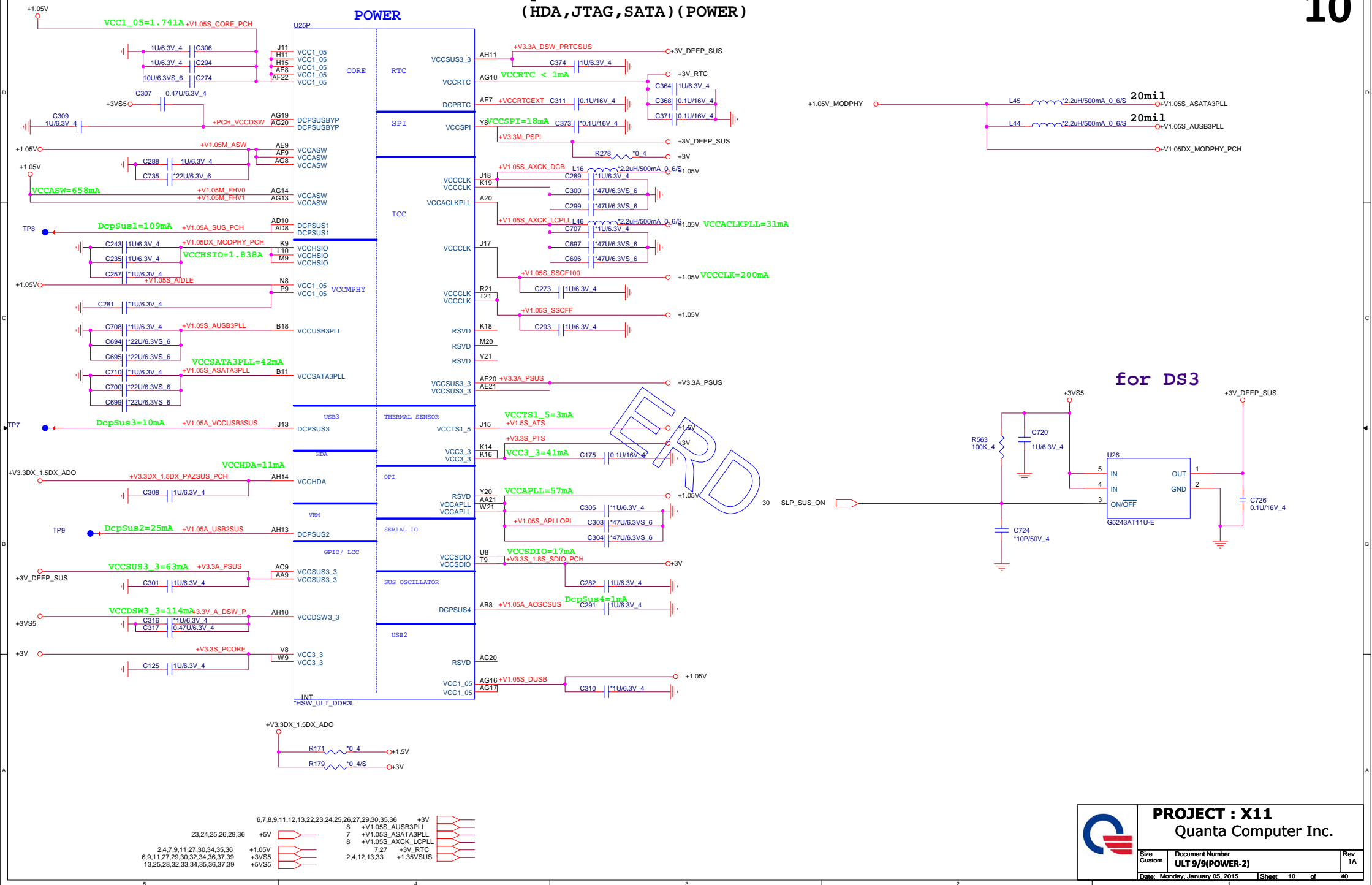
PROJECT : X11
Quanta Computer Inc.

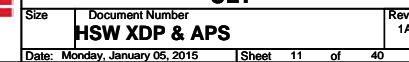
Size Custom	Document Number ULT 7/9 (PCIE/USB/CLK)	Rev 1A
Date: Monday, January 05, 2015	Sheet	8 of 40

09

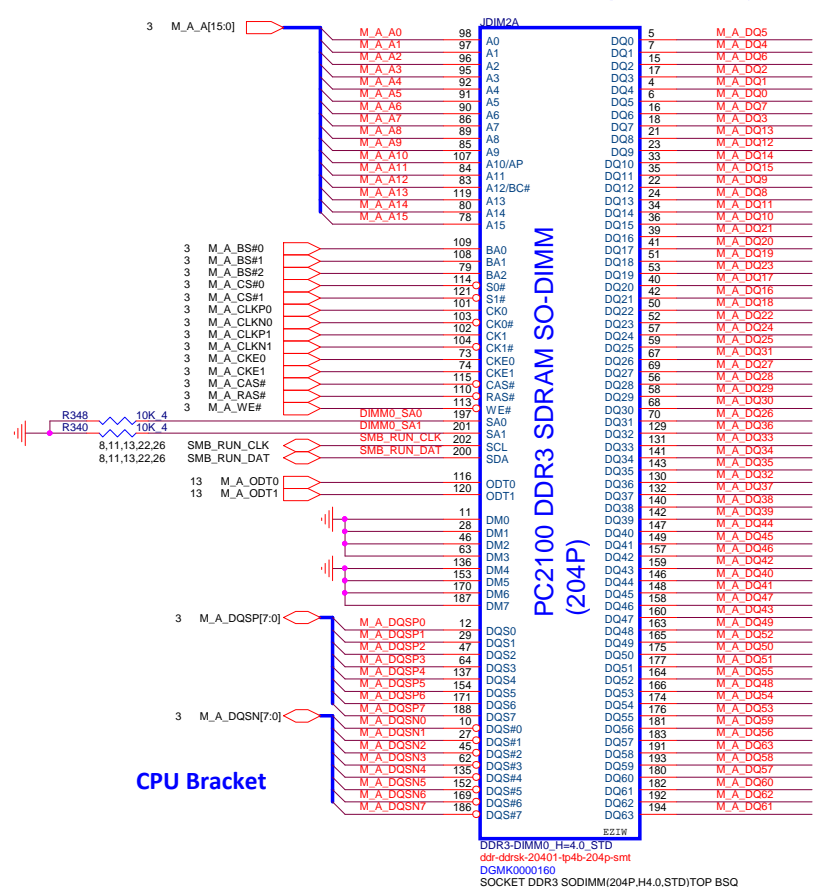


Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) (POWER)



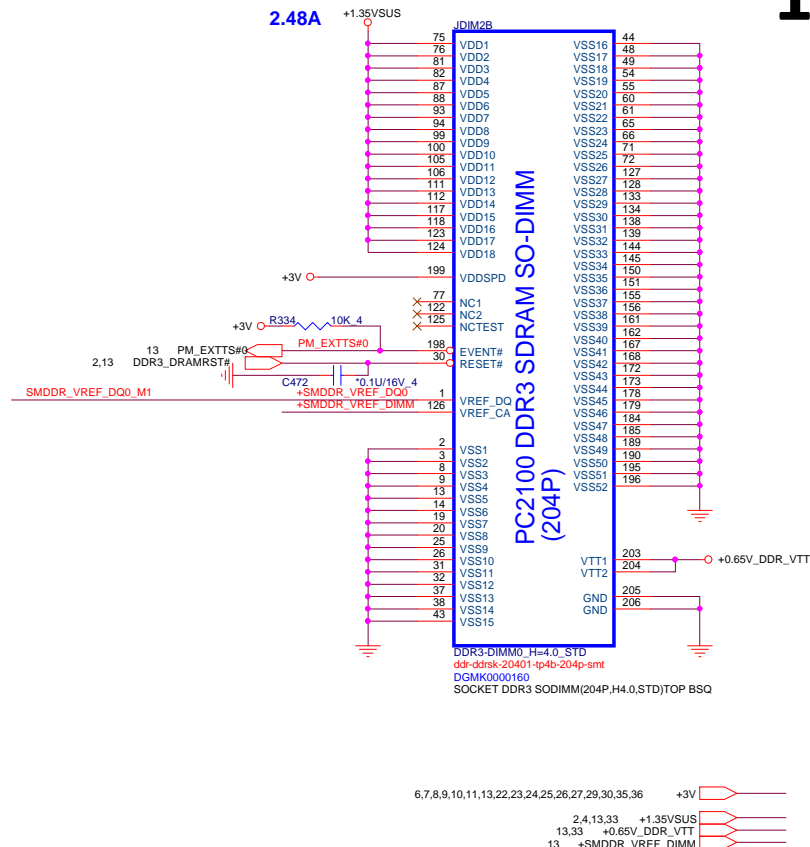


DIMM & Footprint 同Joshua提供



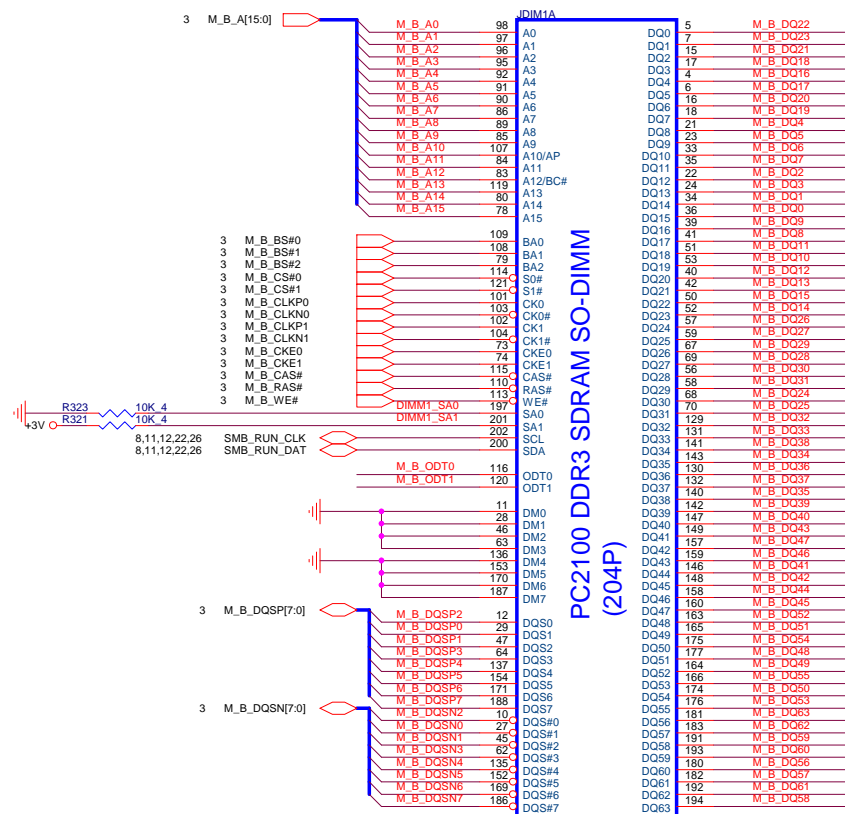
M_A_DQ[63:0] 3

ERD



DIMM & Footprint 同Joshua提供

M_B_DQ[63:0] 3

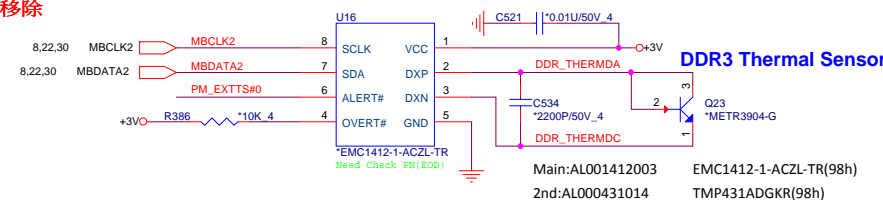


DDR3-DIMM1_H=4.0_RVS
ddr-ddr3k-20401-tp4b-204p-smt
DGMK0000158

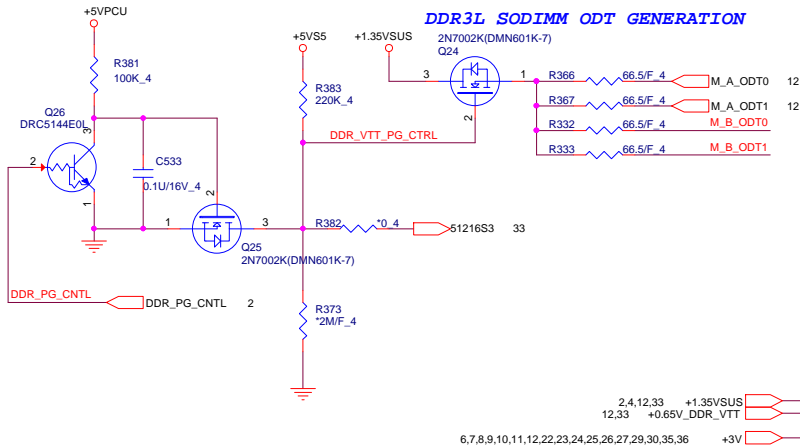


Local Thermal Sensor

mv可移除

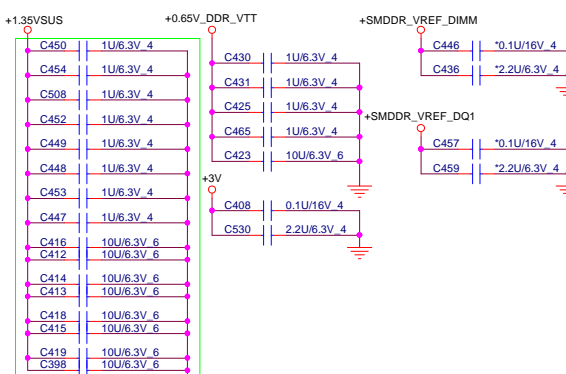


DDR3L SODIMM ODT GENERATION

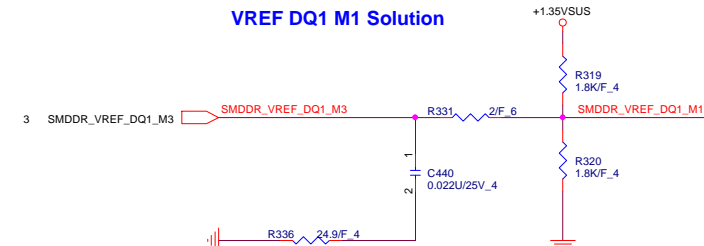


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution

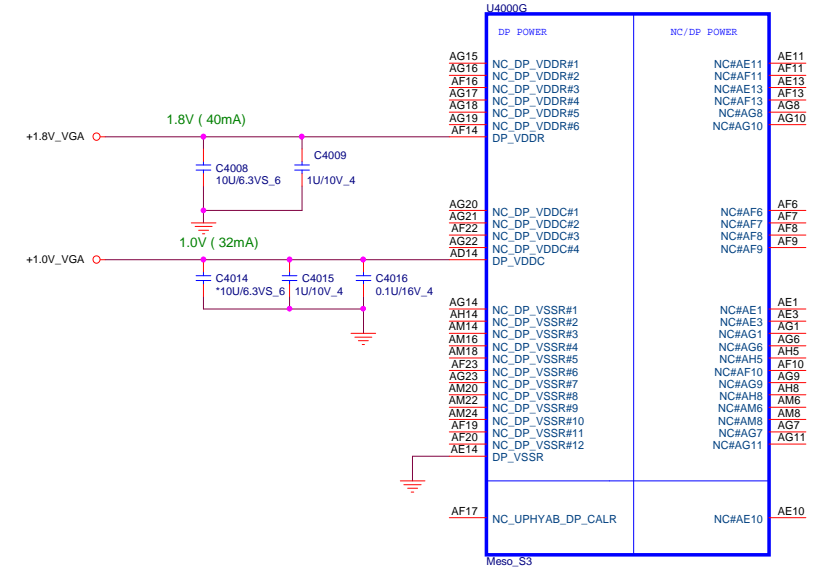
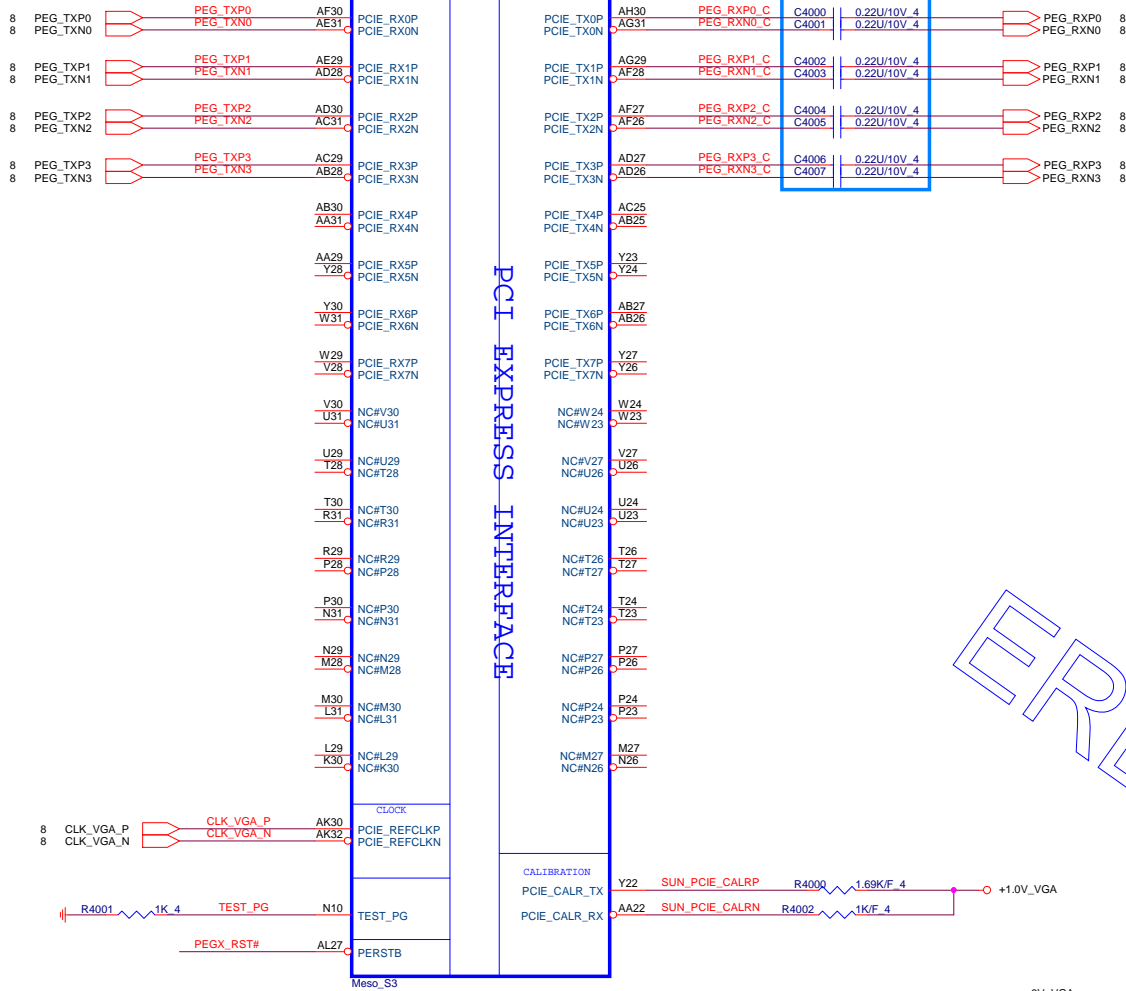


PROJECT : X11
Quanta Computer Inc.

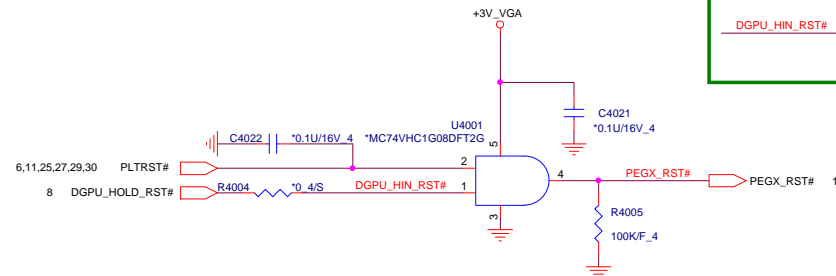
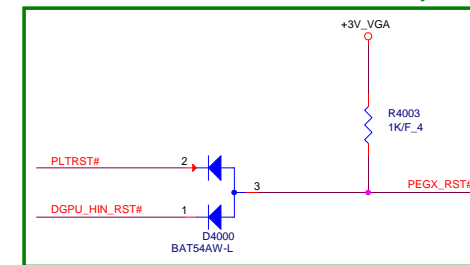
Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A
Date: Monday, January 05, 2015	Sheet	40


Platform	Type	P/N
Carrizo _{HP}	Gen 3	CH4222K9B04 _{RD}
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

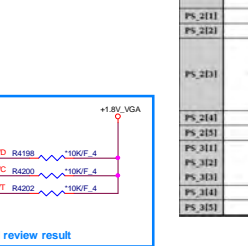
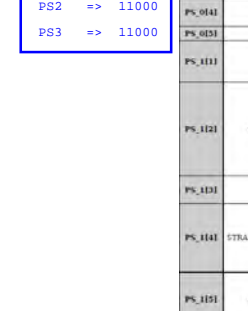
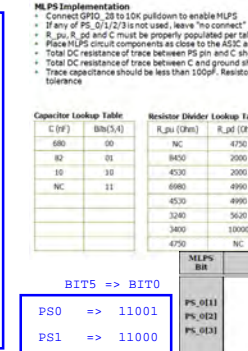
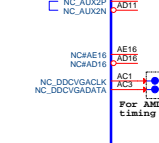
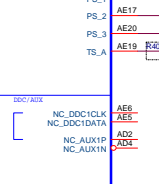
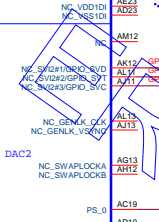
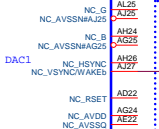
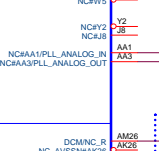
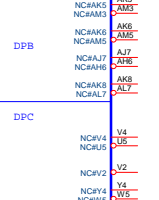
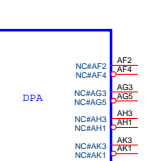
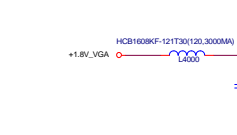
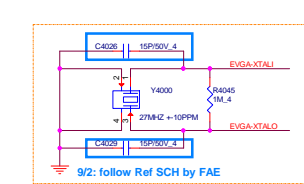
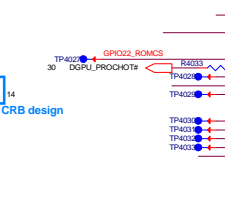
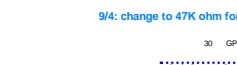
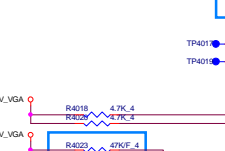
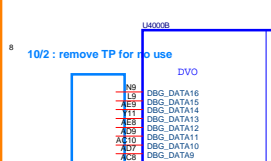
9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)



12/10:reserve for verify



	PROJECT : X11				
	Quanta Computer Inc.				
	Size	Document Number TOPAZ S3 PCIE/DP power			1A
Monday, July 05, 2015	Sheet	14	43	Rev	

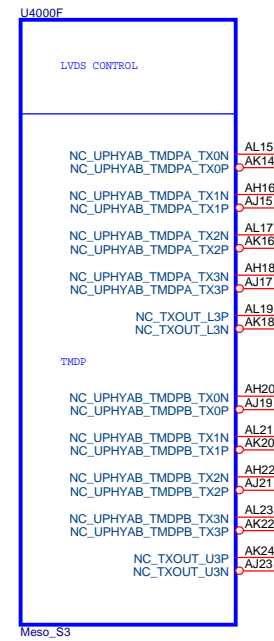
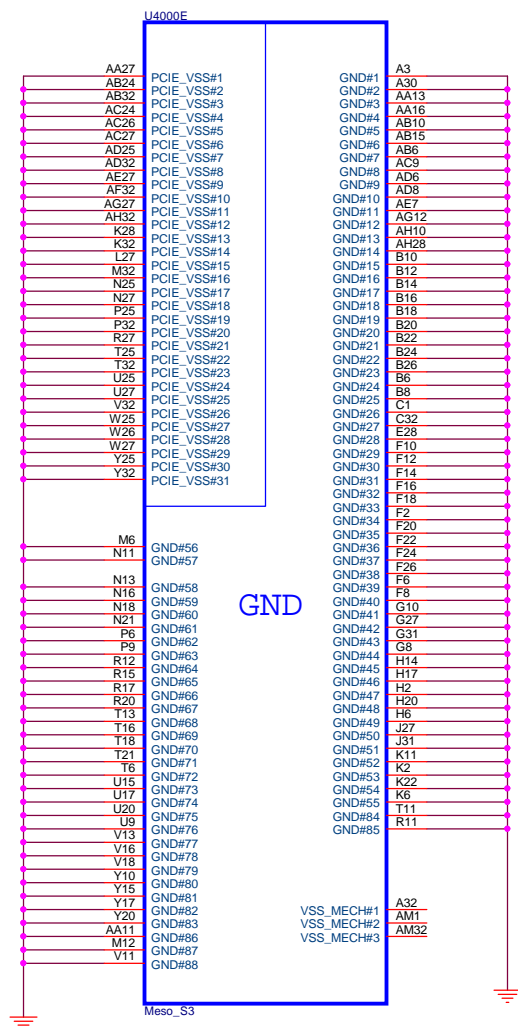


R _{pu} (Ohm)	R _{pd} (Ohm)
NC	4750
8450	2000
4530	2000
6980	4990
4530	4990
3240	5620
3400	10000
4750	NC

PS_0[1]	Ro
PS_0[2]	Ro
PS_0[3]	Ro
PS_0[4]	
PS_0[5]	

Strap Name	Description	Recommended Settings
ROM_CFG0[0]	If STRAP_ROM_EN = 1, ROM_CFG0[0] defines the ROM type.	
ROM_CFG0[1]		Design dependent, see the description.
ROM_CFG0[2]	If STRAP_ROM_EN = 0, ROM_CFG0[2] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 235).	
N/A	Reserved for internal use only.	
	Must be 1 at reset.	1
STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
STRAP_BIF_CLK_PEN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#).	
	0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
N/A	Reserved for internal use only. Must be 0 at reset.	0
CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half swing is enabled. 1 = The transmitter full swing is enabled	1
P_TX_DEEMPH_EN	PCI EXPRESS Tx de-emphasis, transmit-dependent enable. 1 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
N/A	Reserved.	0
N/A	Reserved.	0
STRAP_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
N/A	Reserved.	1
N/A	Reserved.	1
BOARD_CONFIG0	Board configuration related strap, such as for memory ID	Design dependent, see the description.
BOARD_CONFIG1		
BOARD_CONFIG2		
N/A	Reserved.	1
N/A	Reserved.	1

	CS24752FB12
CS28452FB12	CS22002FB19
CS24532FB08	CS22002FB19



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

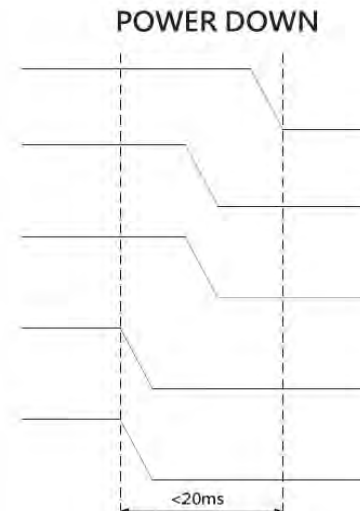
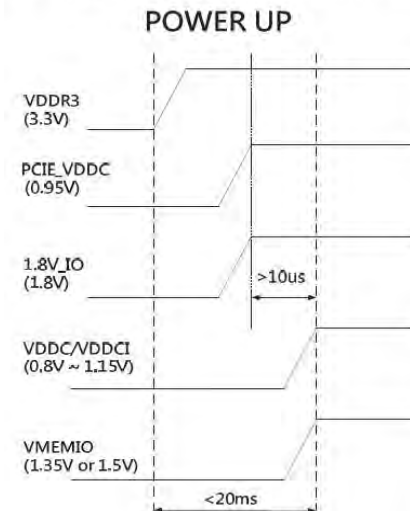
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

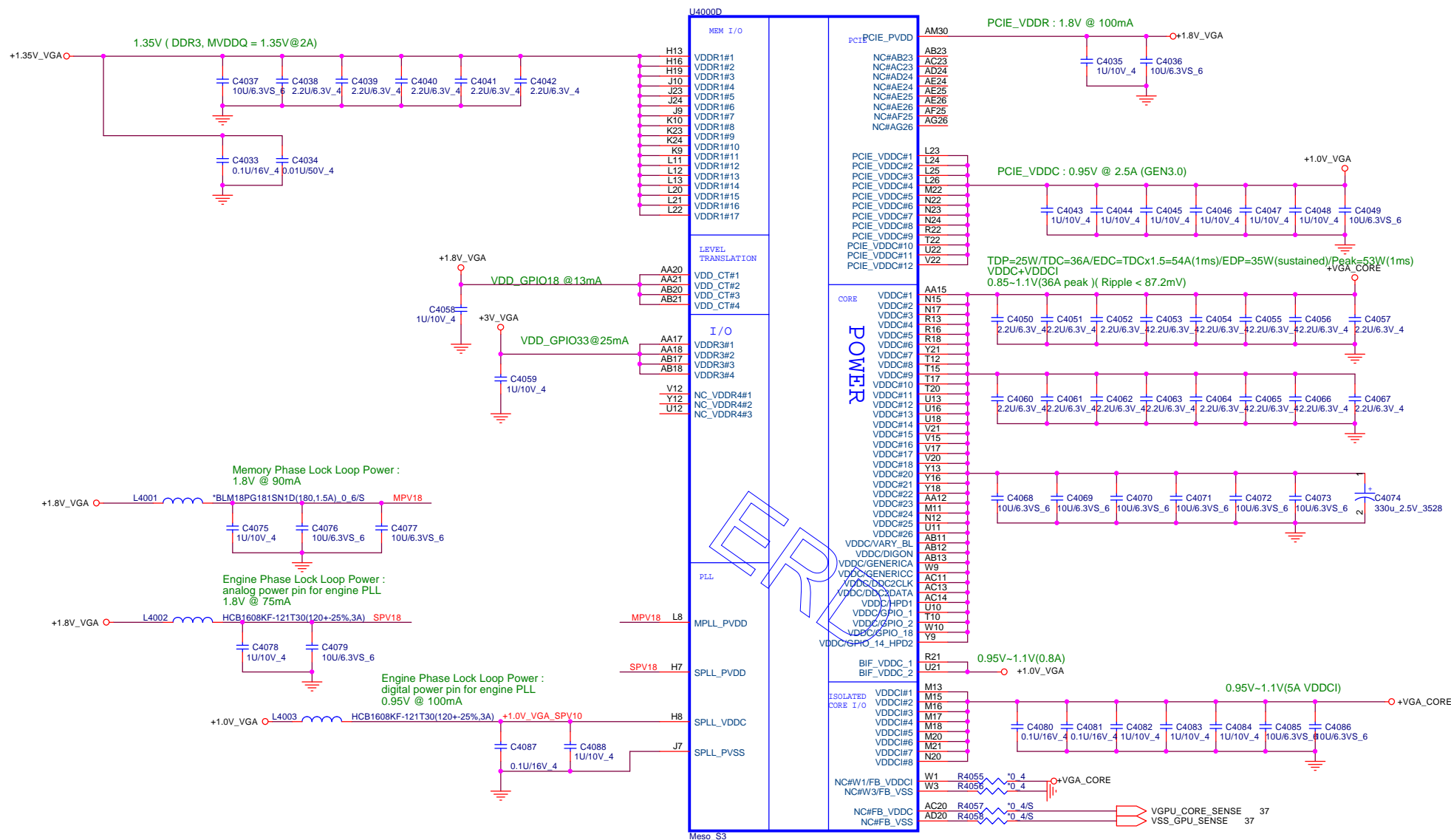
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

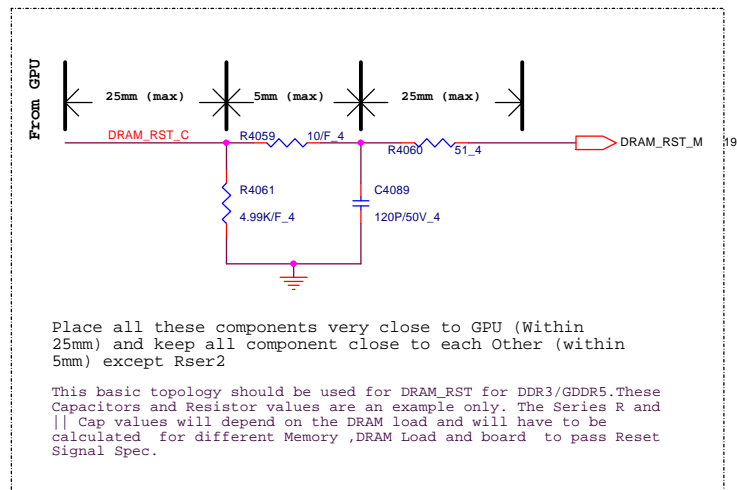


PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date:	Monday, January 05, 2015	Sheet 16 of 43




+	1.35V_VGA	18,19,37
+	1.8V_VGA	14,15,27,37,39
+	1.0V_VGA	14,39
+	VGA_CORE	37,38






ERD



PROJECT : X11
Quanta Computer Inc.

Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	Rev 1A
Date: Monday, January 06, 2018	Sheet	20 of 43

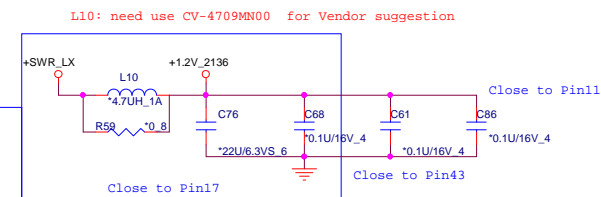
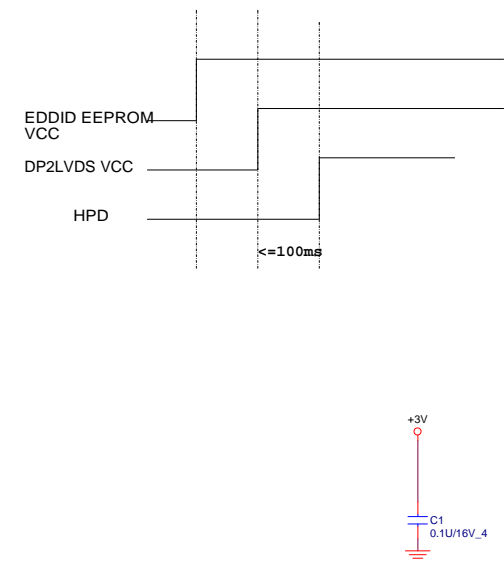
ERD




PROJECT : X11
Quanta Computer Inc.

Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	Rev 1A
Date: Monday, January 05, 2015		Sheet 21 of 43

22



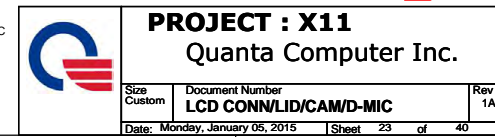
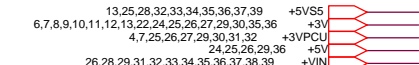
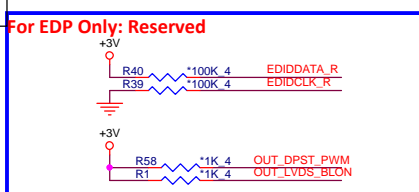
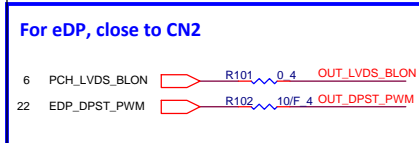
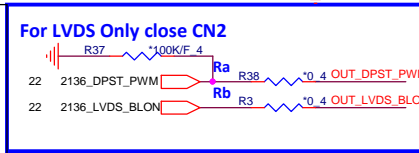
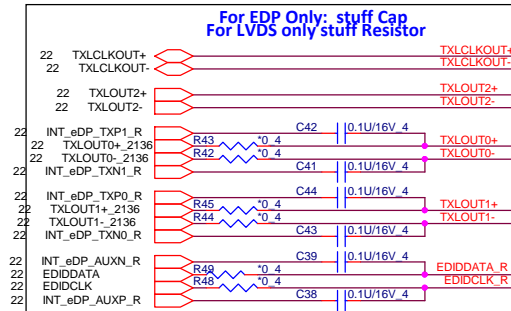
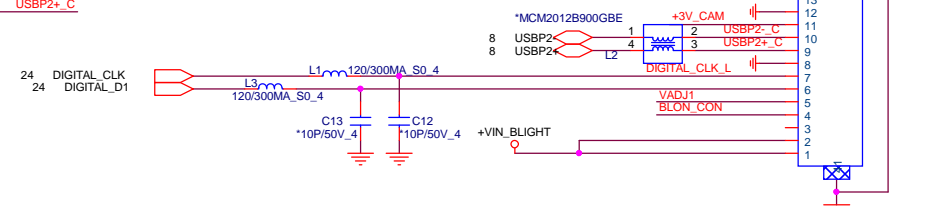
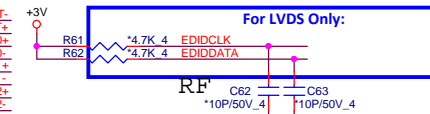
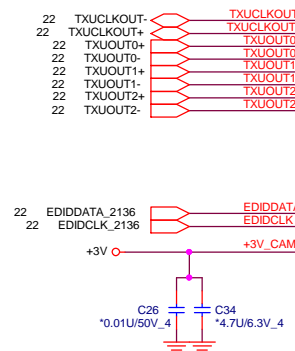
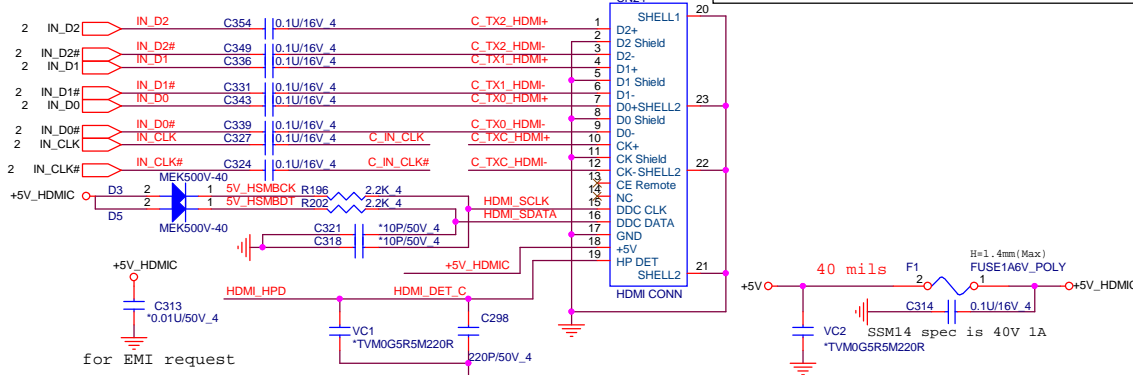
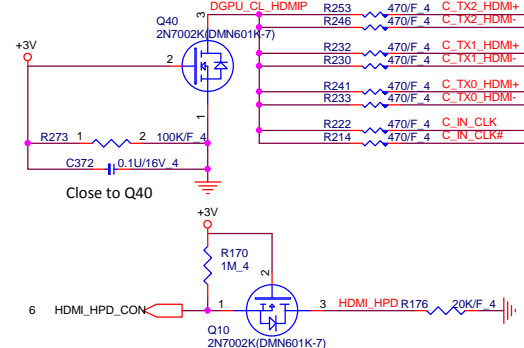
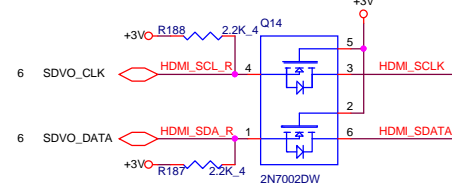
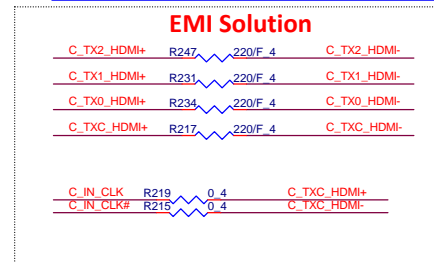
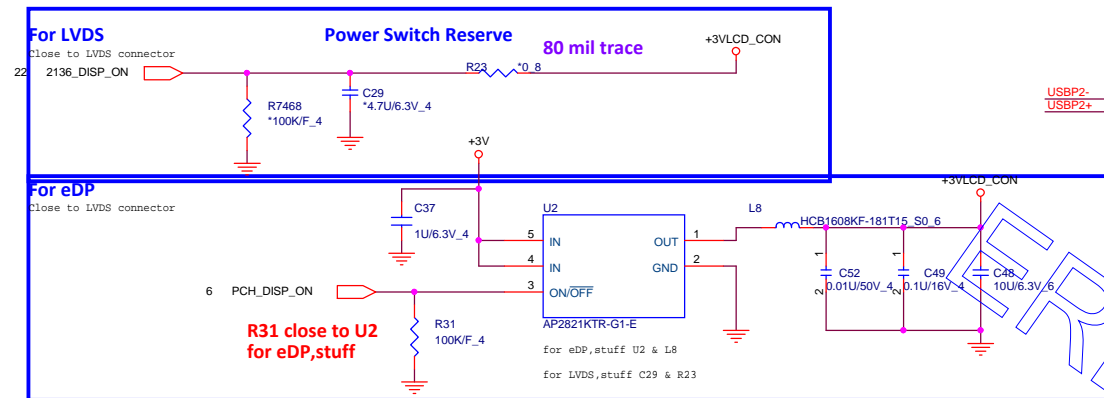
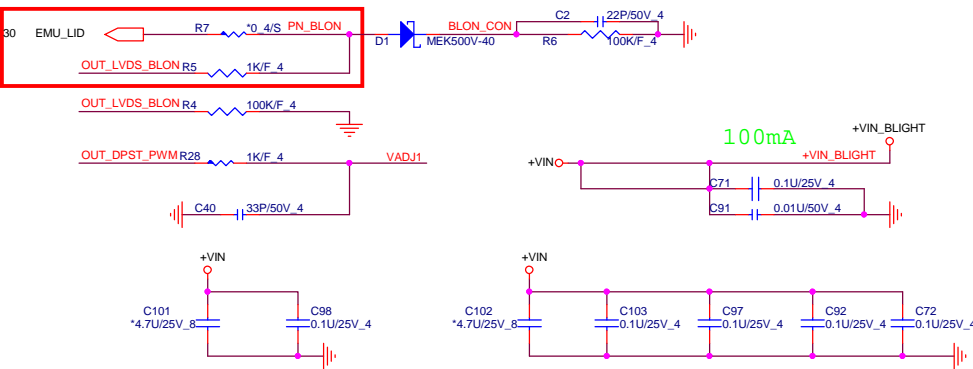


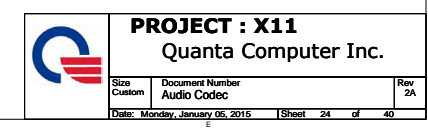
PROJECT : X11

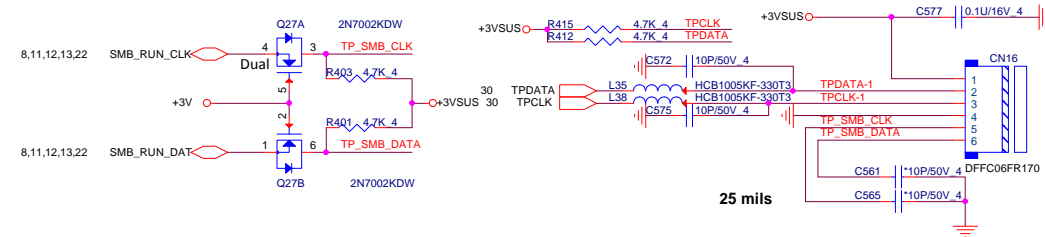
Quanta Computer Inc.

Size Custom	Document Number RTD2136	Rev 1A
Date: Monday, January 06, 2015 Sheet: 23 of 45		

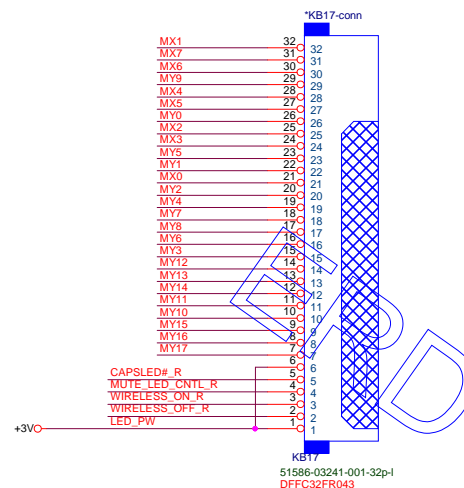
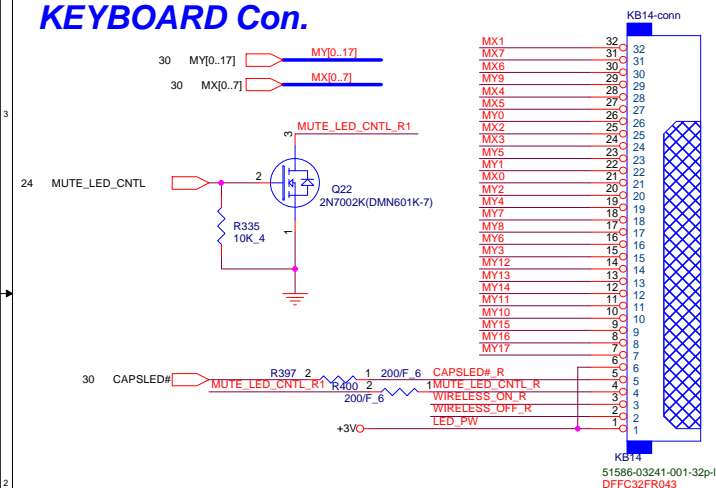
LID Switch



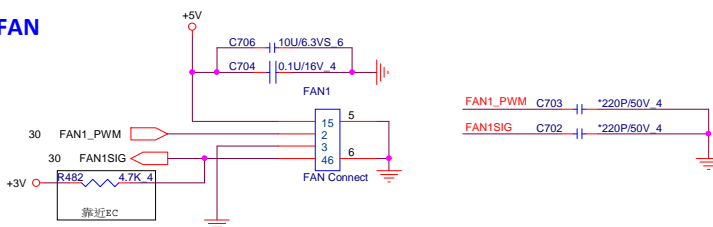




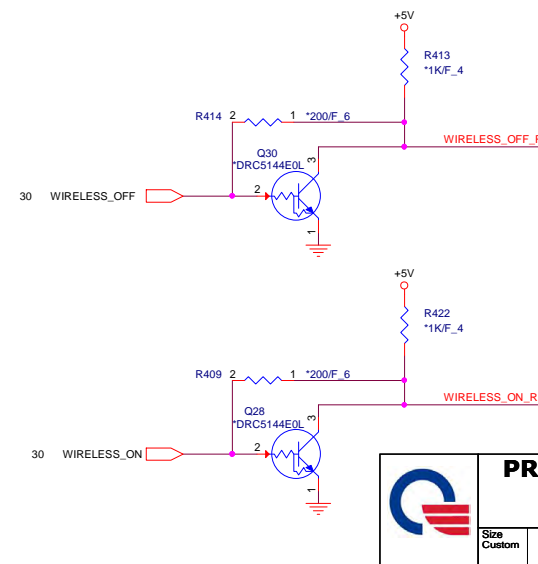
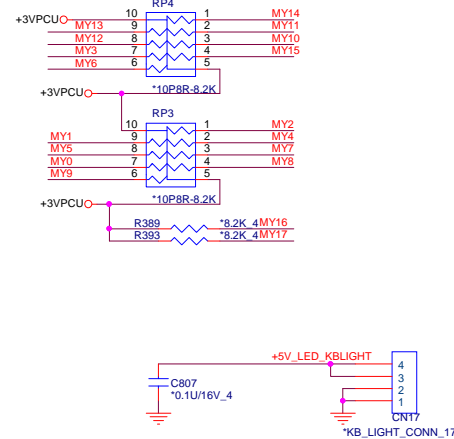
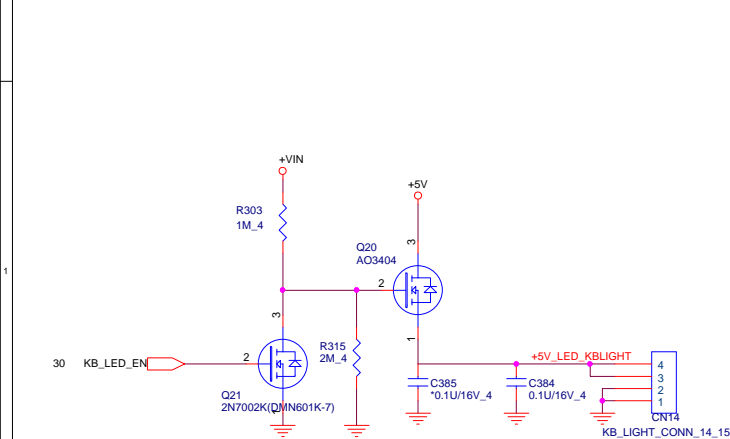
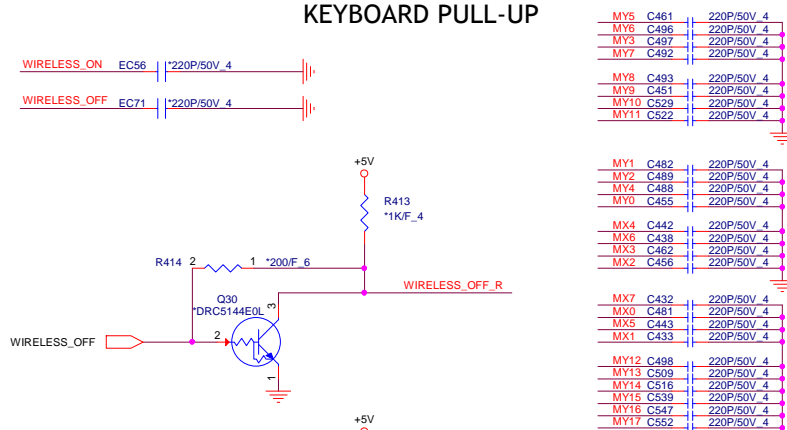
KEYBOARD Con.




FAN



KEYBOARD PULL-UP

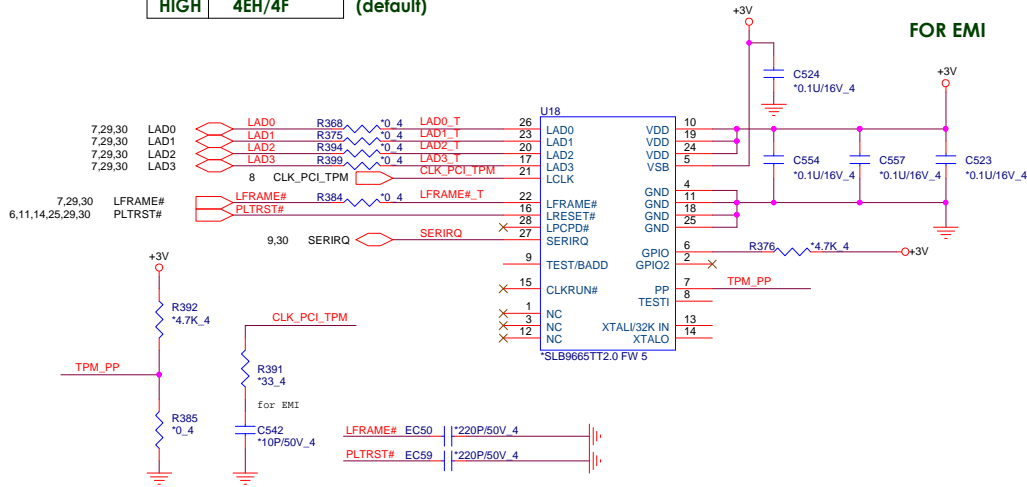


	PROJECT : X11 Quanta Computer Inc.		
	Size Custom	Document Number PB/TP/KB/FAN/EMI Cap	Rev 1A
	Date: Monday, January 05, 2015	Sheet	26 of 40

TPM (2.0)

Address

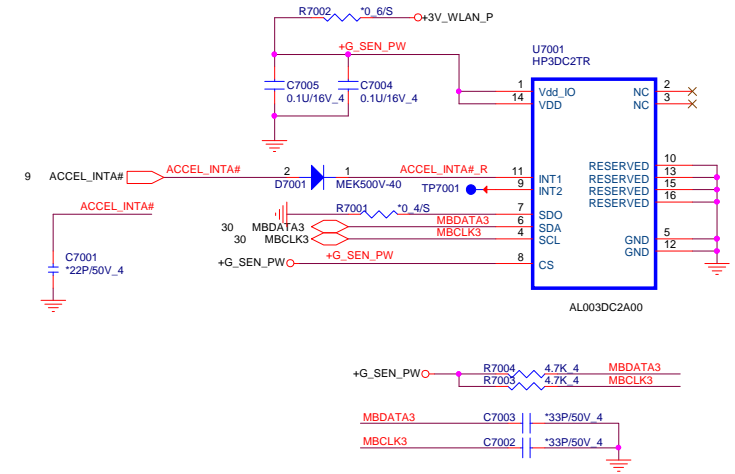
	BADD
HIGH	4EH/4F (default)



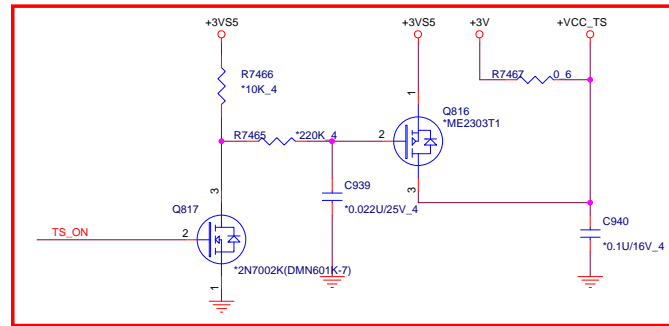
Accelerometer Sensor

27

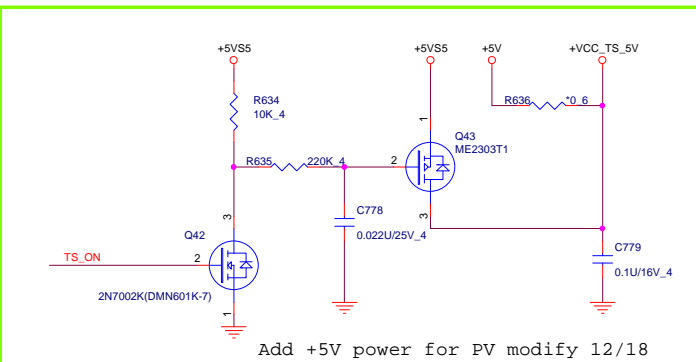
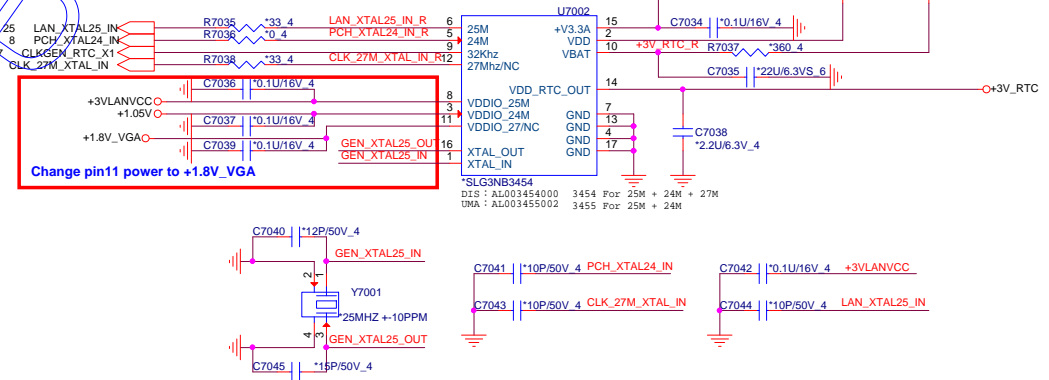
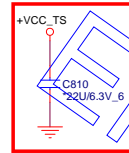
G-Sensor Power need check



Touch screen



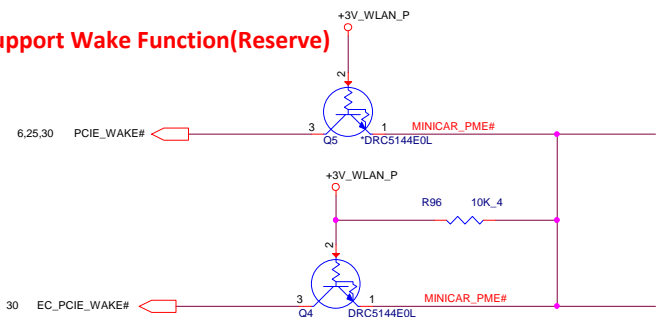
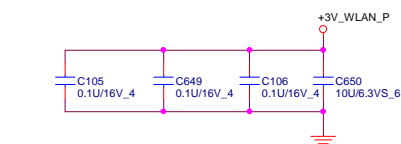
Green CLK Circuitry



Add +5V power for PV modify 12/18

PROJECT : X11		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	TPM/G-Sensor/G-CLK/TS/FP	1A
Date:	Monday, January 05, 2015	Sheet 27 of 40

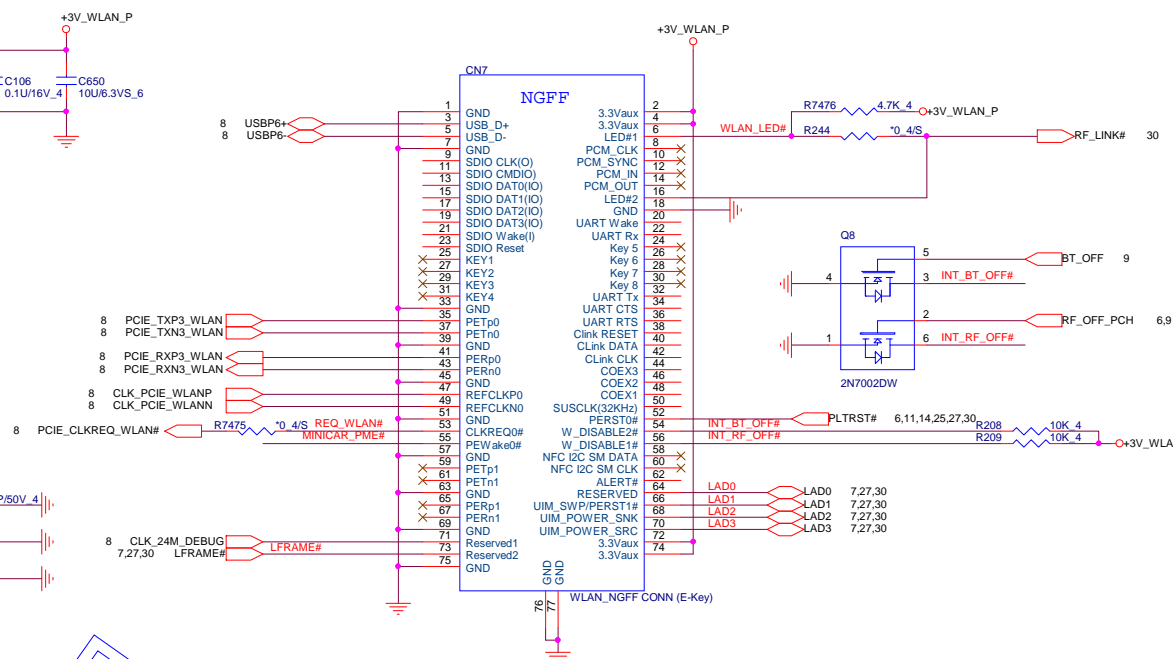
Support Wake Function(Reserve)



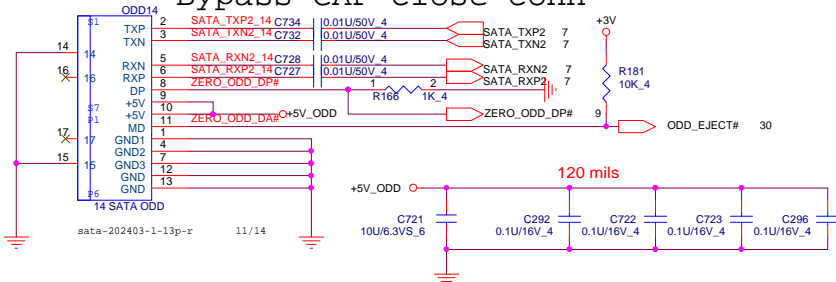
CLK_24M_DEBUG R91 EC10 *33P/50V 4

PCIE_WAKE# EC12 *220P/50V 4

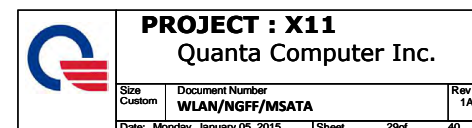
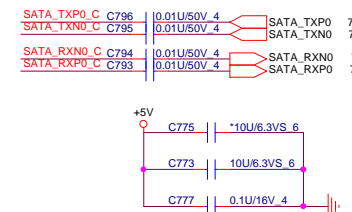
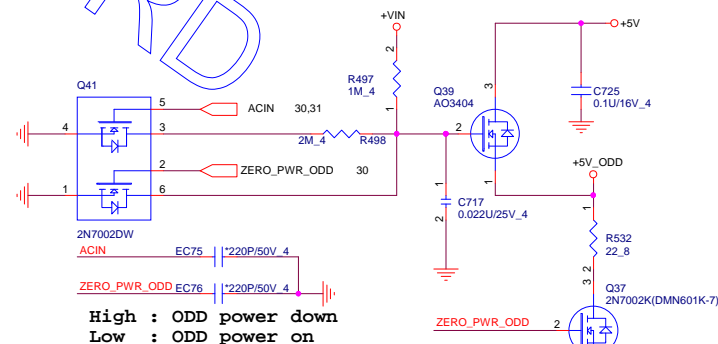
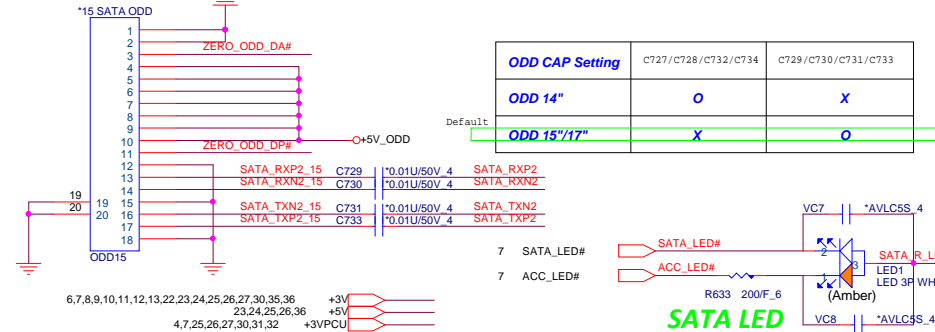
EC_PCIE_WAKE# EC13 *220P/50V 4

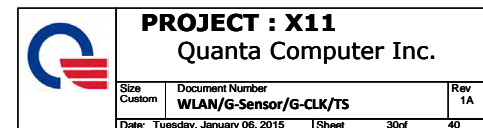


Bypass CAP close conn



*15 SATA ODD

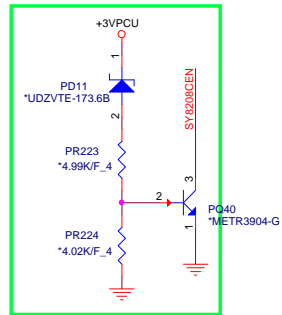
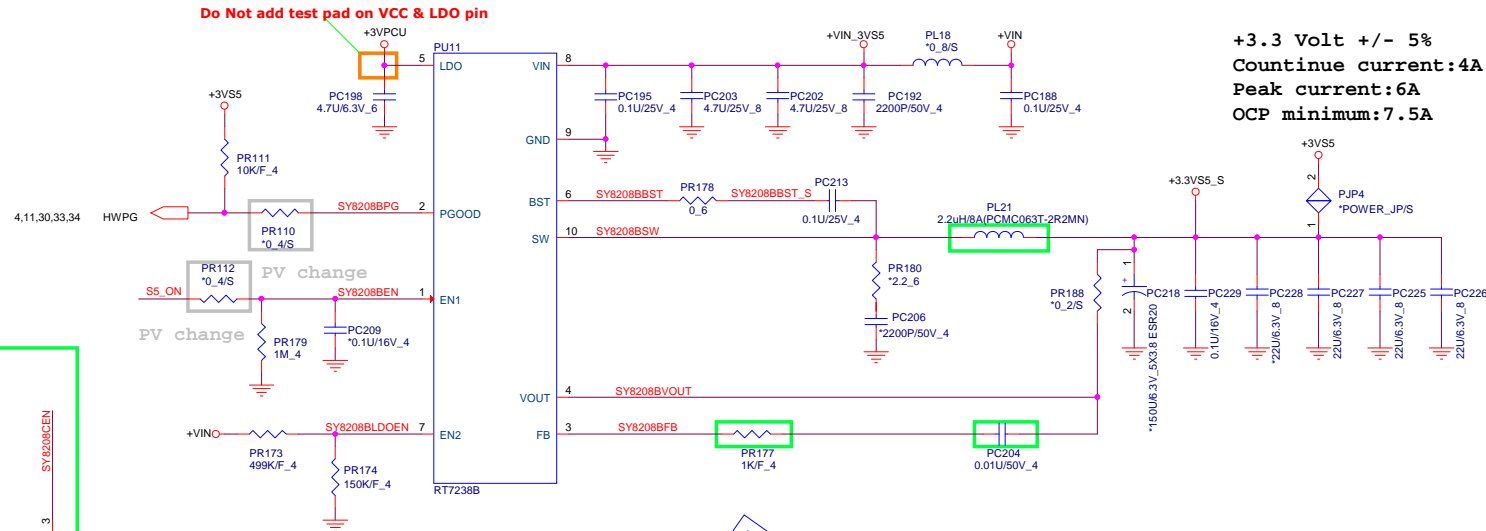






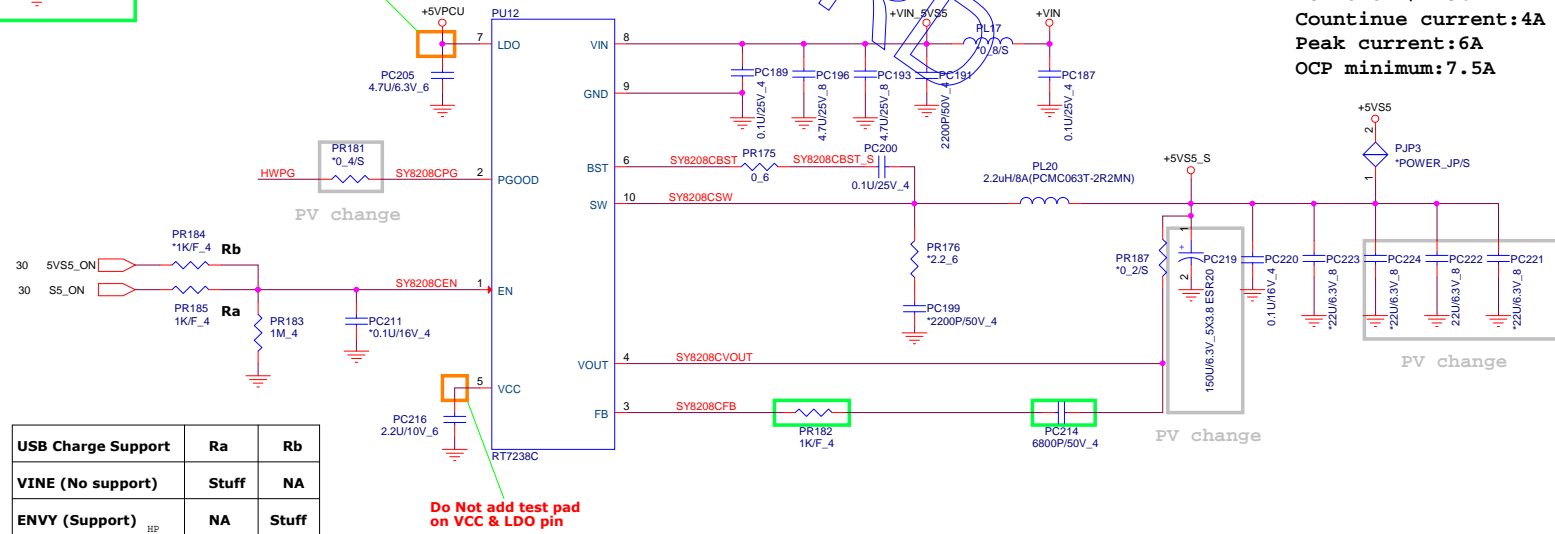
+3VS5 6,9,10,11,27,29,30,34,36,37,39
+5VS5 13,25,28,33,34,35,36,37,39

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



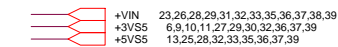
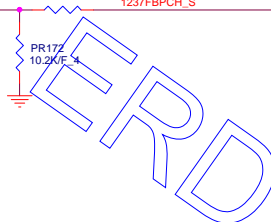
Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

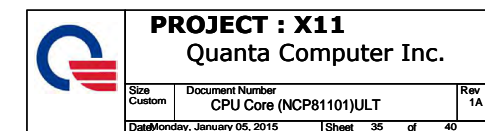


USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

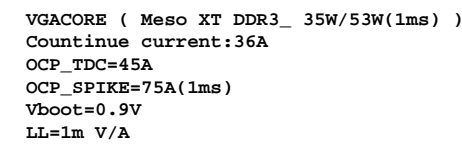
Do Not add test pad on VCC & LDO pin

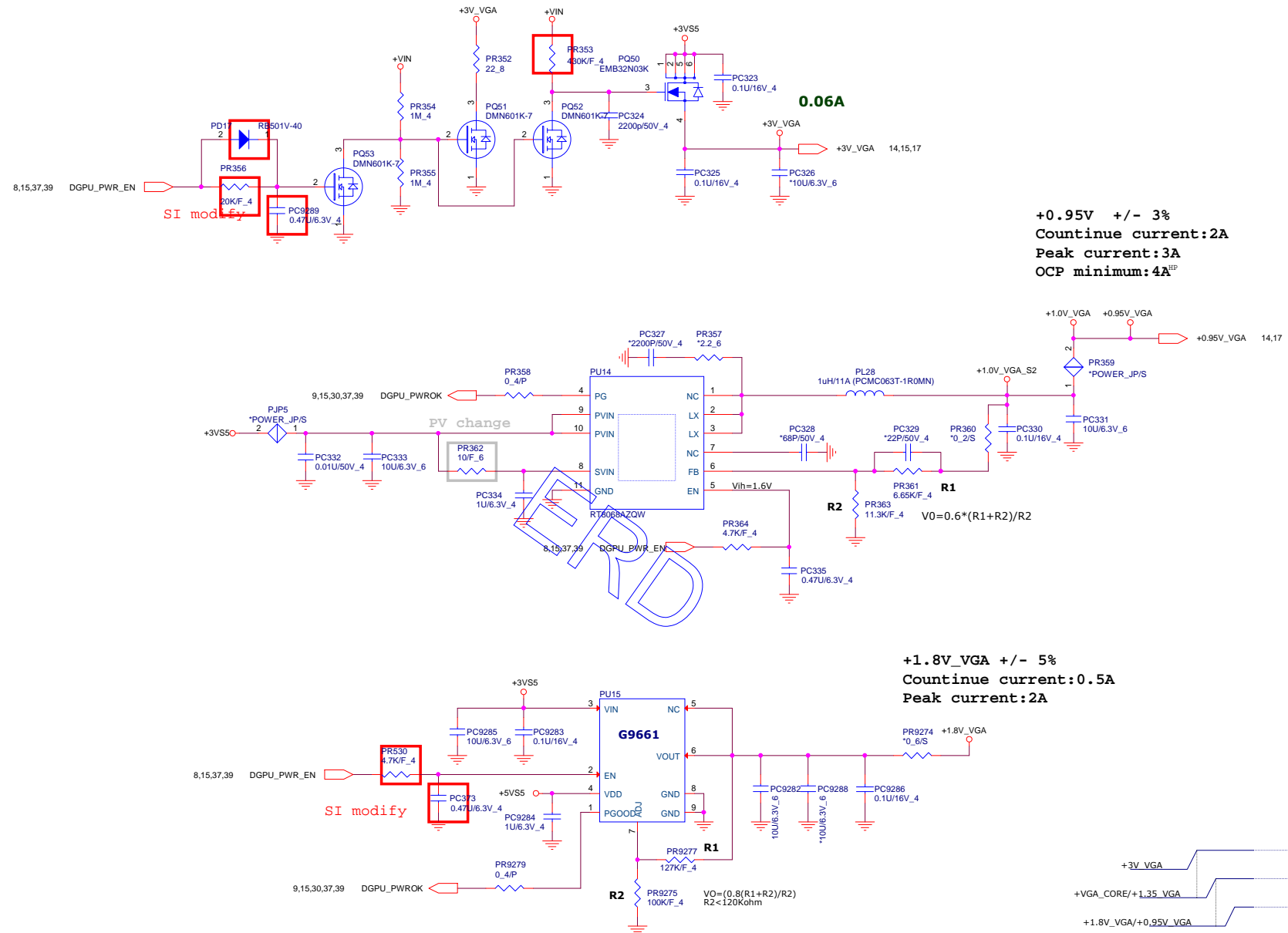


WWW.AliSaler.Com










Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4 、 PC148
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

	PROJECT : X11		
	Quanta Computer Inc.		
	Size	Document Number	Rev
Monday, January 05, 2015		40	40
Date:		Sheet	of